

Google scholar

"array boundary" + (exception OR interrupt) +

Search

Advanced Scholar Search

Scholar

Articles and patents

anytime

include citations

Create email alert

Results 1 - 1 of 1. (0.14 sec)

[\[PDF\] Distribution Diskette](#)

[\[PDF\] from psu.edu](#)

MIT Patch - 1983 - Citeseer

... The reason that a word is IMMEDIATE is normally because it is required to take some compile-time action, for example, LITERAL takes a number from the stack and encloses it, together with the run-time literal **handler**, in the new word so that the number may be returned to the ...

[All 5 versions](#)

Create email alert

"array boundary" + (exception OR in

Search

Google scholar

(condition OR compare) + (branch OR jump) + Search Advanced Scholar Search

Scholar Articles and patents anytime include citations Create email alert

Results 1 - 10 of about 466,000. (0.26 sec)

The 801 minicomputer

[PDF] from psu.edu

G Radin - IBM Journal of Research and Development, 1983 - portal.acm.org

... in favor of high usage of primitive instructions (such as LOAD, STORE, **BRANCH**, **COMPARE**, **ADD**). ... Displacement (signed 16- or 26-bit word offset), or 0 Register + Register, **BRANCH AND LINK** ... branches are defined not only based upon the state of the **Condition** Register but ...

Cited by 343 - Related articles - BL Direct - All 22 versions

Lx: a technology platform for customizable VLIW embedded processing

[PDF] from psu.edu

P Faraboschi, G Brown, JA Fisher... - ACM SIGARCH ..., 2000 - portal.acm.org

... also includes 64 32-bit General- purpose registers and 8 1-bit **branch** registers (used to store **branch condition**, predicates and ... The ISA includes a complete set of **compare** and logic operations and a separate set of 8 1-bit **branch** ... **Branch** Units are restricted only to cluster 0. 206 ...

Cited by 302 - Related articles - BL Direct - All 20 versions

Enhanced **branch** delay slot handling with single **exception program** counter

F Worrell - US Patent 5,774,709, 1998 - Google Patents

... also branches to an **instruction** at a target 55 **instruction** if a test **condition** is true. ... TLB Miss by simply fixing the TLB (Translation Lookaside Buffer) and executing a **Jump** Register to the ... When the computer instructions 45 to move a useful **instruction** from the **branch** target into the ...

Cited by 18 - Related articles - All 2 versions

System for processing single-cycle **branch instruction** in a pipeline having relative, absolute, indirect and trap addresses

BW Case, RG Fleck, CG Kong... - US Patent 4,777,587, 1988 - Google Patents

... To return from the **interrupt** routine then, processor 10 will perform an indirect **jump** via the ... an indirect **jump** via the value saved by the "SAVE—PC-JUMP" **instruction** and will ... delay" **instruction** and a plurality of **branch** instructions each determining a "**branch condition**", stored in ...

Cited by 78 - Related articles - All 2 versions

Formal verification of superscale microprocessors with multicycle functional units, **exception**, and **branch prediction**

[PDF] from psu.edu

MN Velev... - Proceedings of the 37th Annual Design ..., 2000 - portal.acm.org

... For example, an equality comparison of two data operands, as used to deter- mine the **condition** to take a **branch-on-equal instruction**, must be ... A return-from-**exception instruction** has the effect of **jump-** ing to the ExceptionPC and clearing the **exception** status registers. ...

Cited by 99 - Related articles - Library Search - BL Direct - All 15 versions

System for reducing delay for execution subsequent to correctly predicted **branch instruction** using fetch information stored with each block of instructions in cache

WM Johnson - US Patent 5,136,897, 1992 - Google Patents

... This **condition** is required to detect a taken **branch** that was predicted to be not taken. ... If there is an **exception** or **branch** misprediction, the entire contents of the reorder buffer 20 are dis ... the **instruction** block, a dual ported block status array 42 that contains a **branch** block indicator ...

Cited by 226 - Related articles - All 4 versions

[HTML] QEMU, a fast and portable dynamic translator

[HTML] from usenix.org

F Bellard - 2005 - usenix.org

... The **condition code** evaluation is further optimized at translation time by using the fact that the **code** ... On some hosts (such as x86 or PowerPC), a **branch instruction** is directly patched so that the ... longjmp() is used to **jump** to the **exception** handling **code** when an **exception** such as ...

Cited by 526 - Related articles - Cached - All 15 versions

[BOOK] Analysis of **branch** prediction strategies and **branch** target buffer design

[PDF] from berkeley.edu

JKF Lee, AJ Smith... - 1983 - eecs.berkeley.edu

... It is possible if the **condition code** affecting a conditional **branch** has already been determined ... We compare their results to our own as appropriate in the remainder of this paper ... first define two terms: Static **Branch** Instructions - This refers to the individual **branch** instructions found ...

Cited by 589 - Related articles - Library Search - All 12 versions

Machine organization of the IBM RISC System/6000 processor

GF Grohowski - IBM Journal of Research and Development, 2010 - ieeeexplore.ieee.org

... Figures 4(e) and 4(f) depict a taken conditional **branch** whose **condition** is set two fixed ... any pipeline delay are taken conditional branches that depend upon a fixed-point **compare** which cannot be scheduled with three or more instructions between it and the **branch**. ...


Cited by 139 - Related articles - All 8 versions

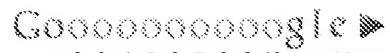
Multi-instruction stream **branch** processing mechanism

JF Hughes, JS Liptay, JW Rymarczyk... - US Patent ..., 1980 - Google Patents

... RETRY CONTROLS 20-1- **INSTRUCTION** PREPROCESSING FUNCTION (IPPF) E-FUNCTION 23 THREE **INSTRUCTION** 21 **STREAM** PRE-FETCH 28 **INSTRUCTION** ^ PRE-DECODE ?q ... 29, 1980 Sheet 6 of 12 4,200,927 BCR Mi R2 **BRANCH** ON **CONDITION** BC MI X2 ...

Cited by 135 - Related articles - All 3 versions

 [Create email alert](#)

Google 

Result Page: [1](#) [2](#) [3](#) [4](#) [5](#) [6](#) [7](#) [8](#) [9](#) [10](#) [Next](#)

[\(condition OR compare\) + \(branch C](#) [Search](#)

[Go to Google Home](#) - [About Google](#) - [About Google Scholar](#)

©2010 Google

Google scholar

array + boundary + (exception OR interrupt) +

Search

[Advanced Scholar Search](#)

Scholar Articles and patents



anytime



include citations

[Create email alert](#)

Results 1 - 10 of about 368,000. (0.19 sec)

ABCD: eliminating array bounds checks on demand[\[PDF\] from psu.edu](#)

R Bodik, R Gupta... - ... of the ACM SIGPLAN 2000 conference ..., 2000 - portal.acm.org
 ... There is one node for each e-SSA-variable, constant, or array-length literal (eg, the value A.length); edge weights constrain the differences ... A **bounds** check can be viewed as a special if statement that will transfer program's control into the **exception handler** if the ...

Cited by 176 - [Related articles](#) - [BL Direct](#) - [All 20 versions](#)**Compiling Java just in time**

T Cramer, R Friedman, T Miller, D Seberger... - Micro, ..., 2002 - ieeeexplore.ieee.org
 ... If the same **array** element is accessed more than once in a basic block, only the first ... Future compilers may perform more advanced analyses to eliminate unnecessary **bounds** checks ... The compiled code for an **exception handler** needs to locate the current values of local variables ...

Cited by 130 - [Related articles](#) - [BL Direct](#) - [All 10 versions](#)**Marmot: An optimizing compiler for Java**[\[PDF\] from psu.edu](#)

R Fitzgerald, TB Knoblock, E Ruf... - Software: Practice ..., 2000 - interscience.wiley.com
 ... and we eventually adopted Freund's minimalist approach of expanding try-finally **handlers** in line. ... yet a widely used technique, particularly in the face of Java's **exception** semantics. Several techniques for **array bounds** check optimization have been developed for Fortran [18–23 ...

Cited by 177 - [Related articles](#) - [BL Direct](#) - [All 27 versions](#)**Overview of the IBM Java just-in-time compiler**[\[PDF\] from iit.edu](#)

T Suganuma, T Ogasawara, M Takeuchi... - IBM Systems ..., 2010 - ieeeexplore.ieee.org
 ... For example, a program may contain an infinitely running loop that exits only through an **array** index out-of-**bounds exception**. ... Once an **exception** of this type has been raised, the system-level **exception handler** directly calls the user-level **handler**, which is registered ...

Cited by 191 - [Related articles](#) - [BL Direct](#) - [All 16 versions](#)**A certifying compiler for Java**[\[PDF\] from iutis.edu](#)

C Colby, P Lee, GC Necula, F Blau... - ACM SIGPLAN ..., 2000 - portal.acm.org
 ... Specifically, we have hoisted and eliminated several null-pointer and **array-bounds** checks ... than the contents of the integer stored at address eax + 4, which is the length of the coefficients **array**. ... ure 5) shows that an **exception handler** is a 5-word structure, stored on the run-time ...

Cited by 227 - [Related articles](#) - [BL Direct](#) - [All 25 versions](#)**Implementing jalapeño in Java**[\[PDF\] from docjava.com](#)

B Alpern, CR Attanasio, A Cocchi... - Proceedings of the ..., 1999 - portal.acm.org
 ... below the virtual machine rather than above it, Jalapeño reduces the **boundary-crossing** overhead ... When these values are stored in the boot-image **array**, it is written to ... **Exception Handling** - The **exception handler** (like the garbage collector) uses the memory access facilities to ...

Cited by 257 - [Related articles](#) - [BL Direct](#) - [All 9 versions](#)**Automated test-data generation for exception conditions**[\[PDF\] from psu.edu](#)

N Tracey, J Clark, K Mander... - Software: Practice and ..., 2000 - interscience.wiley.com
 ... Constraint Error exceptions occur when a value goes out of range; examples include type **bounds**, **array bounds**, arithmetic underflow/overflow and attempts to divide by zero. ... The problem of structural test coverage of the **exception handler** is addressed in a similar manner. ...

Cited by 82 - [Related articles](#) - [BL Direct](#) - [All 22 versions](#)**Java bytecode to native code translation: the caffeine prototype and preliminary results**

CHA Hsieh, JC Gytiierhaat... - ... of the 29th annual ACM/IEEE ..., 1996 - portal.acm.org
 ... can be captured by the try-block's **handler**. Fourth, for maximum portability, **exception** handling support in the Java interpreter does not rely on the underlying architecture or operating system. Thus, the interpreter explicitly checks for null references, **array index bounds**, divide by ...

Cited by 99 - [Related articles](#) - [BL Direct](#) - [All 4 versions](#)**Processor with accelerated array access bounds checking**

M Tremblay, JM O'Connor... - US Patent 6,014,723, 2000 - Google Patents
 ... in the C programming language, and instead has true arrays in which **array bounds** are explicitly checked, thereby eliminating vulnerability to many viruses and nasty bugs. The JAVA programming language includes objective-C interfaces and specific **exception handlers**. ...

Cited by 51 - [Related articles](#) - [All 4 versions](#)**Design, implementation, and evaluation of optimizations in a just-in-time compiler**[\[PDF\] from psu.edu](#)

K Ishizaki, M Kawahito, T Yasue... - Proceedings of the ..., 1999 - portal.acm.org
 ... rs : Check **array-bounds** multi r4, 14. 2 1wzx l-3. r4cr5, i Get **array** element twi LLT, l-7. 1 ; Check divisor divi r3, r3, 1-7 The **handler** void TrapHandler(struct context l cp) int *iar = cp-SIAR; // Get the address a~ which // the **exception** occurs if IS_TRAPI-EQ(iar ...

Cited by 89 - [Related articles](#) - [BL Direct](#) - [All 32 versions](#) [Create email alert](#)



Result Page: 1 [2](#) [3](#) [4](#) [5](#) [6](#) [7](#) [8](#) [9](#) [10](#) [Next](#)

array + boundary + (exception OR ir [Search](#)

[Go to Google Home](#) - [About Google](#) - [About Google Scholar](#)

©2010 Google

Google scholar

[Advanced Scholar Search](#)
Scholar

Results 1 - 10 of about 244. (0.24 sec)

Processor with accelerated array access bounds checking

M Tremblay, JM O'connor... - US Patent 6,014,723, 2000 - Google Patents

... The **array boundary** check- ing apparatus of the invention includes an associative memory element that stores and retrieves a plurality of array bound values. ... The JAVA programming language includes objective-C interfaces and specific **exception handlers**. ...

Cited by 51 - [Related articles](#) - [All 4 versions](#)**[PDF] OpenJIT Backend Compiler**

K Shimura - 1998 - openjit.org

... function name description arrayCheck check **array boundary** resolveClass for anewarray, multianewarray, checkcast, instanceof resolveField for putfield, getfield ... it can be detected inside of compiled code or runtime routines and thrown to appropriate **exception handler**. ...

Cited by 3 - [Related articles](#) - [View as HTML](#)[\[PDF\] from openill.org](#)**[CITATION] Exception Handling**

N Ryan

[Related articles](#)**Programmable IC with gate array core and boundary scan capability**

GA Baxter, KB Buch... - US Patent 6,226,779, 2001 - Google Patents

... An **exception** to this rule is when the FPGA configuration process did not involve other parts of the system (eg, configuration was under the control of the FPGA), in which case configuration can sometimes be skipped without affect- ing system functionality. ...

Cited by 12 - [Related articles](#) - [All 2 versions](#)**Hardware/software optimization for array & pointer boundary checking against buffer overflow attacks**

Z Shao, J Cao, KCC Chan, C Xue... - Journal of Parallel and ..., 2006 - Elsevier

... **Exception** SignalFig. 4. The implementation of the special bound checking instruction in DLX.take advantage of the special boundary checking instruction to optimize the performance.The previous software optimization mainly focuses on opti- mizing **array boundary** ...

Cited by 1 - [Related articles](#) - [All 12 versions](#)[\[PDF\] from psu.edu](#)**Robust two-dimensional weighted and unweighted phase unwrapping that uses fast transforms and iterative methods**

DC Ghiglia... - Journal of the Optical Society of ..., 1994 - opticsinfobase.org

... The rewrapped val- ues depicted in Fig. 2 are shown in Fig. 3 and are quali- tatively consistent (with the possible **exception** of an in- consequential constant bias) with the original input depicted in Fig. 1. Because the original input was noise Fig. ...

Cited by 401 - [Related articles](#) - [Bk Direct](#) - [All 10 versions](#)**A floating point rectangular systolic array on a chip**

RJ Clarke, JA Curtis, AP Clarke... - Automation towards the ..., 2002 - ieeexplore.ieee.org

... The use of serial data both minimises the I/O pin count at the **array boundary** and allows adjacent processing elements to both ... 2.3.4 **Exception** Processing: IEEE encoded data is processed according to IEEE standards with the **exception** of some rounding modes, and the ...

Cited by 1 - [Related articles](#)**System and method for low overhead boundary checking of java arrays**

LC Goff, DR Evoy... - US Patent 6,782,407, 2004 - Google Patents

... a system- to the array to get blocked, and a read access to the array to data cache 30 and **array boundary** checker 50. get effectively ignored. In addition, the same error signal The Local-Variable memory 20 includes high perfor- 15 also causes an **Exception** Status register in a ...

Cited by 1 - [Related articles](#) - [All 4 versions](#)**[BOOK] OKI advanced array processor (AAP) hardware description**

BR Musicus, GNS Prasanna... - 1991 - mit.dspace.org

... 50 5.8. Micro-Interrupt System 51 5.9. ... individually programmable direction select possible via SL register bits, but data transfer not supported at **array boundary**. - only 3 sixteen bit busses available, limiting transfer capabilities, ...

[View as HTML](#) - [Library Search](#) - [All 6 versions](#)[\[PDF\] from dspace.org](#)**Memory device and method for redundancy/self-repair**

B Cleveland, A Ilkhanian... - US Patent App. 10/ ..., 2001 - Google Patents

... The memory device 40 also comprises read/write control 60, an **exception handler** 70, a row decoder 80, and a redundant row decoder 90. [0025] In operation, the read/write control 60 attempts to write data in the primary memory array 52 at a given address. ...

Cited by 4 - [Related articles](#) - [All 4 versions](#)

"array boundary" + (exception OR in [Search](#)

[Go to Google Home](#) - [About Google](#) - [About Google Scholar](#)

Google scholar

"array boundary" + (exception OR interrupt) + Search Advanced Scholar Search

Scholar Articles and patents anytime include citations Create email alert

Results 1 - 10 of about 16. (0.23 sec)

Processor with accelerated array access bounds checking

M Tremblay, JM O'Connor... - US Patent 6,014,723, 2000 - Google Patents

... The **array boundary** check- ing apparatus of the invention includes an associative memory element ...
 j?4 1M CACHE .330 INSTRUCTS DECODER V131 || **BRANCH** , WIDE ' NDEX ... The JAVA
 programming language includes objective-C interfaces and specific **exception handlers**. ...

Cited by 51 - Related articles - All 4 versions

[PDF] OpenJIT Backend Compiler

K Shimura - 1998 - openjit.org

... nop **branch** call return tblsw ret ... function name description arrayCheck check **array boundary**
 resolveClass for anewarray, checkcast, instanceof resolveField for ... detected inside
 of compiled code or runtime routines and thrown to appropriate **exception handler**. ...

Cited by 3 - Related articles - View as HTML

[\[PDF\] from openjit.org](#)**[PS] Survey of Buffer-Overflow Protection**

K Pirornsopa... - cse.msu.edu

... Control data can be divided into several types: return addresses, function pointers, and **branch**
 slots. ... All n&ffrs **Exception** Function Virtual methods Other Var Function return add res execution
 flow EBP."4 ..^ int i) { T void fune(char i— int j = 0; J C Foo foo ; (* fp) (int) = & fune char ...

Cited by 2 - Related articles

[\[PS\] from msu.edu](#)**Search-based software test data generation: A survey**

P McMinn - Software Testing, Verification and Reliability, 2004 - interscience.wiley.com

... The condition determining whether a **branch** is taken is referred to as the **branch** predicate. ...
 A use of a variable v is a node in which v is referenced, for example in an assignment
 statement, an output statement, or a **branch** predicate expression. ...

Cited by 346 - Related articles - BL Direct - All 19 versions

[\[PDF\] from psu.edu](#)**[PDF] Improving Branch Predictability in Java Processing**

T Li, LK John... - 2001 - Citeseer

... Our analysis [Li01] shows that the highly biased **branch** site distribution, combined
 with the abundance of runtime **exception** checking codes (eg, class verifier and
array boundary checking) that are seldom taken, lead ...

Related articles - View as HTML - All 3 versions

[\[PDF\] from psu.edu](#)**[PDF] Optimising Java Programs Through Basic Block Dynamic Compilation**

IA Rogers - 2002 - cs.man.ac.uk

... 3Some JIT compilers, such as LaTTe [LYK+99], do not translate **exception** handling regions of
 code as they assume they are infrequently executed. Page 19. ... The first basic block performs the
 array creation and loop initialisation, then it performs an unconditional **branch** to the ...

Cited by 2 - Related articles - View as HTML - All 2 versions

[\[PDF\] from man.ac.uk](#)**[PDF] RDB: A system for incremental replay debugging**

MW Shapiro - Master's thesis, Department of Computer Science, ..., 1997 - Citeseer

... of a program in order to detect particular types of program errors, such as memory access
 violations, memory leaks, or **array boundary** violations. ... The instrumentation library's signal **handler**
 then maps a new page of anonymous memory in at the virtual memory page boundary ...

Cited by 6 - Related articles - View as HTML - All 7 versions

[\[PDF\] from psu.edu](#)**Graphical display of complex information within a Prolog debugger**

AD Dewar... - International Journal of Man-Machine Studies, 1986 - Elsevier

... options be set or unset for a particular instance of a call, nor to **interrupt** asynchronously in ... left
 or lower-right corner of the display of that array (ie when an **array boundary** element is ... high-level
 goal, and moving down the right-most 514 AD DEWAR AND JG CLEARY **branch** of its ...

Cited by 36 - Related articles - All 6 versions

[\[PDF\] from ucalgary.ca](#)**[PDF] Evolutionary search for test data in the presence of state behaviour**

P McMinn - 2005 - Citeseer

... A number of experiments show the value of the approach for both test objects with states and
 test objects with input-output behaviour. For all test objects considered, higher levels of **branch**
 coverage are obtained. i Page 4. ... 61 2.5.2 **Exception** Condition Testing

Cited by 10 - Related articles - View as HTML - Library Search - All 6 versions

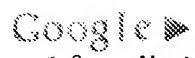
[\[PDF\] from psu.edu](#)**[BOOK] Optimal Path Queries in Very Large Spatial Databases**

J Zhang... - 2005 - Citeseer

Page 1. Optimal Path Queries in Very Large Spatial Databases by Jie Zhang A thesis presented
 to the University of Waterloo in fulfillment of the thesis requirement for the degree of Master of
 Mathematics in Computer Science Waterloo, Ontario, Canada, 2005 c Jie Zhang, 2005 ...

Related articles - View as HTML - Library Search - All 12 versions

[\[PDF\] from psu.edu](#) Create email alert



Result Page: 1 2 [Next](#)

"array boundary" + (exception OR in [Search](#))

[Go to Google Home](#) - [About Google](#) - [About Google Scholar](#)

©2010 Google

Google scholar

(condition OR compare) + (branch OR jump OR

Search

[Advanced Scholar Search](#)

Scholar Articles and patents



anytime



include citations

[Create email alert](#)

Results 1 - 10 of about 530,000. (0.29 sec)

[The 801 minicomputer](#)[\[PDF\] from psu.edu](#)

G Radin - IBM Journal of Research and Development, 1983 - portal.acm.org

... in favor of high usage of primitive instructions (such as LOAD, STORE, **BRANCH**, **COMPARE**, **ADD**). ... Displacement (signed 16- or 26-bit word offset), or 0 Register + Register, **BRANCH AND LINK** ... branches are defined not only based upon the state of the **Condition** Register but ...

[Cited by 343](#) - [Related articles](#) - [BL Direct](#) - [All 22 versions](#)[Lx: a technology platform for customizable VLIW embedded processing](#)[\[PDF\] from psu.edu](#)

P Faraboschi, G Brown, JA Fisher... - ACM SIGARCH ..., 2000 - portal.acm.org

... also includes 64 32-bit General- purpose registers and 8 1-bit **branch** registers (used to store **branch condition**, predicates and ... The ISA includes a complete set of **compare** and logic operations and a separate set of 8 1-bit **branch** ... **Branch** Units are restricted only to cluster 0. 206 ...

[Cited by 302](#) - [Related articles](#) - [BL Direct](#) - [All 20 versions](#)[Enhanced branch delay slot handling with single exception program counter](#)

F Worrell - US Patent 5,774,709, 1998 - Google Patents

... also branches to an **instruction** at a target 55 **instruction** if a test **condition** is true. ... TLB Miss by simply fixing the TLB (Translation Lookaside Buffer) and executing a **Jump** Register to the ... When the computer instructions 45 to move a useful **instruction** from the **branch** target into the ...

[Cited by 18](#) - [Related articles](#) - [All 2 versions](#)[System for processing single-cycle branch instruction in a pipeline having relative, absolute, indirect and trap addresses](#)

BW Case, RG Fleck, CG Kong... - US Patent 4,777,537, 1988 - Google Patents

... and will perform an indirect **jump** via the value saved by the "SAVE—PC—JUMP" **instruction** and will ... at step (d) and the contents of said **program** counter, based on said **branch condition** saved at ... pipeline during a cycle next-fol- lowing a cycle during which said **branch** delay was ...

[Cited by 78](#) - [Related articles](#) - [All 2 versions](#)[Formal verification of superscale microprocessors with multicycle functional units, exception, and branch prediction](#)[\[PDF\] from psu.edu](#)

MN Velev... - Proceedings of the 37th Annual Design ..., 2000 - portal.acm.org

... For example, an equality comparison of two data operands, as used to deter- mine the **condition** to take a **branch-on-equal instruction**, must be ... A return-from-**exception instruction** has the effect of **jump-** ing to the ExceptionPC and clearing the **exception** status registers. ...

[Cited by 59](#) - [Related articles](#) - [Library Search](#) - [BL Direct](#) - [All 15 versions](#)[Mechanism for implementing one machine cycle executable trap instructions in a primitive instruction set computing system](#)

MA Auslander, J Cocke, HT Hao... - US Patent ..., 1996 - Google Patents

... Architecture Conference Proceedings It is a primary object of the present invention to pro- vide a 'trap' **instruction** and mechanism ... of a primitive reduced **instruction** set machine system, as compared to several machine cycles of a **compare** and **branch condition** sequence on ...

[Cited by 23](#) - [Related articles](#) - [All 2 versions](#)[System for reducing delay for execution subsequent to correctly predicted branch instruction using fetch information stored with each block of instructions in cache](#)

WM Johnson - US Patent 5,136,697, 1992 - Google Patents

... This **condition** is required to detect a taken **branch** that was predicted to be not taken. ... If there is an **exception** or **branch** misprediction, the entire contents of the reorder buffer 20 are dis ... the **instruction** block, a dual ported block status array 42 that contains a **branch** block indicator ...

[Cited by 226](#) - [Related articles](#) - [All 4 versions](#)[\[HTML\] QEMU, a fast and portable dynamic translator](#)[\[HTML\] from unix.org](#)

F Bellard - 2005 - unix.org

... The **condition code** evaluation is further optimized at translation time by using the fact that the **code** ... On some hosts (such as x86 or PowerPC), a **branch instruction** is directly patched so that the ... longjmp() is used to **jump** to the **exception** handling **code** when an **exception** such as ...

[Cited by 526](#) - [Related articles](#) - [Cached](#) - [All 16 versions](#)[\[BOOK\] Analysis of branch prediction strategies and branch target buffer design](#)[\[PDF\] from berkeley.edu](#)

JKF Lee, AJ Smith... - 1983 - eecs.berkeley.edu


... It is possible if the **condition code** affecting a conditional **branch** has already been determined ... We **compare** their results to our own as appropriate in the remainder of this paper ... first define two terms: **Static Branch Instructions** - This refers to the individual **branch** instructions found ...

[Cited by 569](#) - [Related articles](#) - [Library Search](#) - [All 12 versions](#)[Machine organization of the IBM RISC System/6000 processor](#)

GF Grohoski - IBM Journal of Research and Development, 2010 - ieeeexplore.ieee.org

... Figures 4(e) and 4(f) depict a taken conditional **branch** whose **condition** is set two fixed ... any pipeline delay are taken conditional branches that depend upon a fixed-point **compare** which cannot be scheduled with three or more instructions between it and the **branch**. ...

[Cited by 139](#) - [Related articles](#) - [All 8 versions](#)

 [Create email alert](#)



Result Page: [1](#) [2](#) [3](#) [4](#) [5](#) [6](#) [7](#) [8](#) [9](#) [10](#) [Next](#)

[Go to Google Home](#) - [About Google](#) - [About Google Scholar](#)